ABSTRACT

A semiconductor integrated circuit including a logic circuit is disclosed, in which the decoder area can be reduced and which has an effect of reduction of the whole chip size. Among the MOS FETs included in the logic circuit, those other than a MOS FET for supplying electric charges via an output terminal have threshold voltage values lower than the threshold voltage value of the MOS FET for supplying electric charges. The direction of the gate width of each MOS FET is perpendicular to the direction along which word lines extend in the memory cell areas, and all of the MOS FETs are aligned in a direction perpendicular to the direction along which the word lines extend.